URN etd-0407109-183722-1827
Author Chen-Kai Chang
Author's Email Address No Public.
Statistics This thesis had been viewed 42 times. Download 0 times.
Department
Year 2005
Semester 1
Degree Master
Type of Document Master's Thesis
Language zh-TW.Big5 Chinese
Title An Efficient Hardware Architecture of CAVLC for H.264
Date of Defense 0000-00-00
Page Count 91
Keyword
CAVLC
H.264

Abstract
In H.264/AVC, the Context-Based Adaptive Variable Length Coding (CAVLC) is adopted for lossless compression. The low-cost VLSI implementation for CAVLC is discussed in this paper. We use two smaller tables instead a huge codeword table adopted by most traditional methods. The codeword representative pseudo codeword and their valid bit-width are stored in the first smaller table. In the second table, we store the necessary codeword classes and their offset values. Since our design can reduce a lot of memory size, so it is very suitable for low-cost applications.
Advisory Committee Yu-Pin Chang - advisor

Files No Any Full Text File.
Date of Submission 2006-08-04